SINGLE SCAN CHAIN IN HIERARCHIACALLY BISTED DESIGNS

Abstract of Invention

Disclosed are novel methods and apparatus for efficiently providing a single scan chain design for hierarchically BISTed designs. In an embodiment, a method of providing a single scan chain of a chip is disclosed. The method includes: selecting a TOP chain of the chip, the chip being divided into a plurality of embedded logic test (ELT) blocks; bypassing periphery flops of the plurality of ELT blocks; selecting a single scan chain of all ELT blocks of the chip; and inserting the single scan chain of all ELT blocks of the chip into the TOP chain of the chip.